Fig. 1

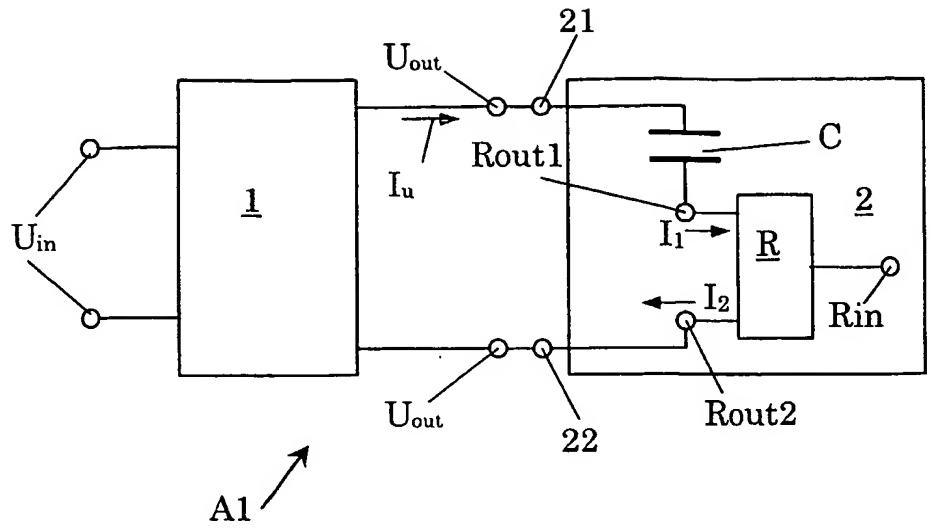

21
Uout
C
Rout1
Iu
1
2
Uin
I1
R
I2
Rin
Uout
22
Rout2
A1

Fig. 2

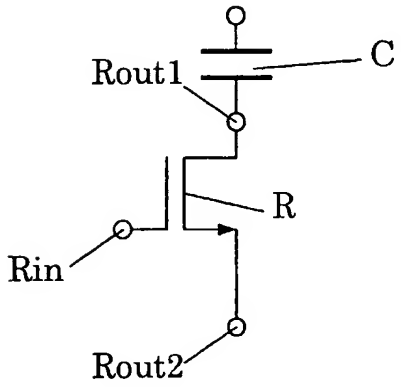

C
Rout1
R
Rin
Rout2

Fig. 3

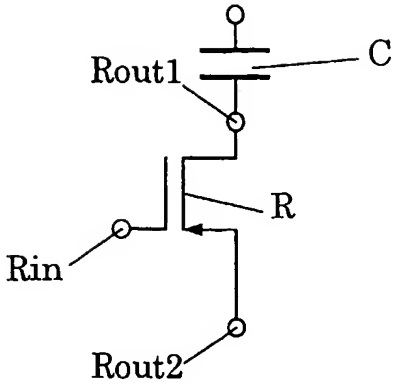


Fig. 4

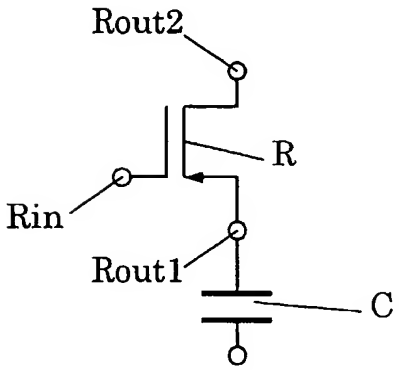


Fig. 5

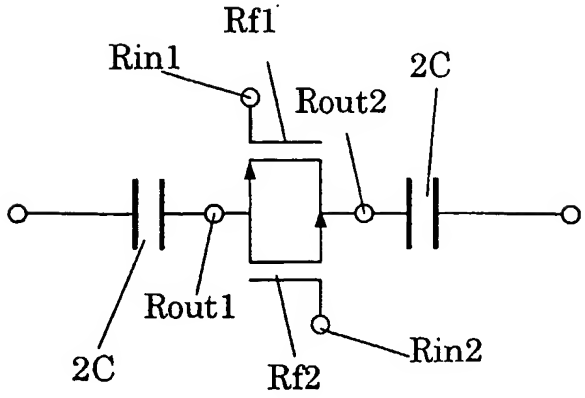


Fig. 6

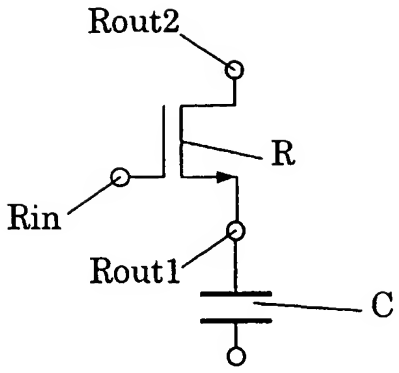


Fig. 7

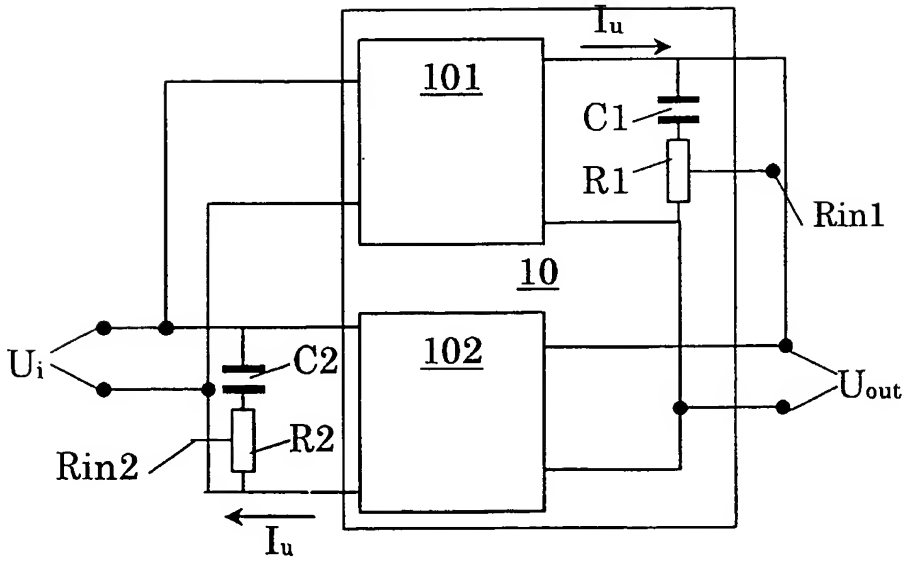


Fig. 8

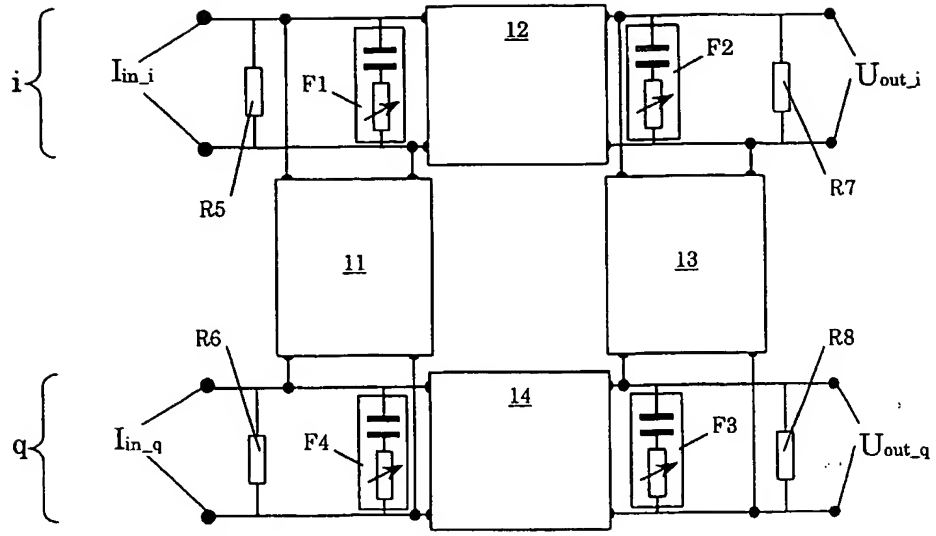
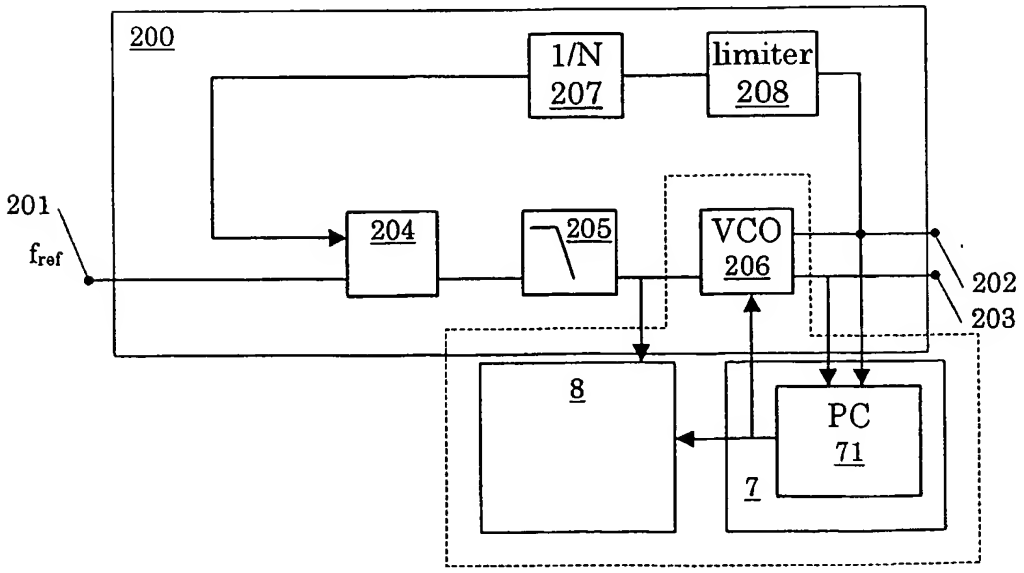

i
I_{in_i}
F1
12
F2
U_{out_i}
R5
R7
11
13
R6
R8
q
I_{in_q}
F4
14
F3
U_{out_q}

Fig. 9


200
1/N
207
limiter
208
201
f_{ref}
204
205
VCO
206
202
203
8
PC
71
7